EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L2	0	(substrate or semiconductor or wafer or carrier or chip) near9 (trench$4 or via$4 or hole$4 or opening$4) and (porous near4 silicon) and (buried near4 cavit$4) and epitax$4 and (dielectric or oxide or insulat$4) and (438/142.ccls.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/30 10:27
L3	1	(substrate or semiconductor or wafer or carrier or chip) near9 (trench$4 or via$4 or hole$4 or opening$4) and (porous near4 silicon) and (buried near4 cavit$4) and epitax$4 and (dielectric or oxide or insulat$4) and (438/197.ccls.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/30 10:34
L4	0	(substrate or semiconductor or wafer or carrier or chip) near9 (trench$4 or via$4 or hole$4 or opening$4) and (porous near4 silicon) and (buried near4 cavit$4) and epitax$4 and (dielectric or oxide or insulat$4) and (257/288.ccls.)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/30 10:34
S1	0	((semiconductor or substrate or wafer or chip) near8 (trench$2)) and cavity and anneal$4 and epitaxy and silicon and porous and transistor and tranducer and microphone	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/30 08:16
S2	0	((semiconductor or substrate or wafer or chip) near8 (trench$2)) and cavity and anneal$4 and transistor and tranducer and microphone	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/10/13 08:13
S3	554	((semiconductor or substrate or wafer or chip) near8 (trench$2)) and cavity and anneal$4 and transistor	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/10/13 08:13
S4	2	((semiconductor or substrate or wafer or chip) near8 (trench$2)) and cavity and anneal$4 and transistor and microphone	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/10/13 08:13

EAST Search History

S5	62	((semiconductor or substrate or wafer or chip) near8 (trench$2)) and cavity and anneal$4 and transistor and transducer	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/10/13 08:13
S6	62	((semiconductor or substrate or wafer or chip) near8 (trench$2)) and cavity and anneal$4 and transistor and transducer and (dielectric or oxide)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/10/13 08:14
S7	6	((semiconductor or substrate or wafer or chip) near8 (trench$2)) and cavity and anneal$4 and transistor and transducer and (dielectric or oxide) and epitaxy	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/10/13 08:14
S8	0	((semiconductor or substrate or wafer or chip) near8 (trench$2)) and cavity and anneal$4 and transistor and transducer and (dielectric or oxide) and (nitrogen near8 atmosphere)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/10/13 08:14
S9	0	((semiconductor or substrate or wafer or chip) near8 (trench$2)) and cavity and anneal$4 and transistor and transducer and (dielectric or oxide) and (argon near8 atmosphere)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/10/13 08:15
S10	0	((semiconductor or substrate or wafer or chip) near8 (trench$2)) and cavity and anneal$4 and transistor and transducer and (dielectric or oxide) and (helium near8 atmosphere)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/10/13 08:15
S11	36	((semiconductor or substrate or wafer or chip) near8 (trench$2)) and cavity and anneal$4 and transistor and transducer and (dielectric or oxide) and (argon or nitrogen or xenon or helium)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/10/13 08:15
S12	0	((semiconductor or substrate or wafer or chip) near8 (trench$2)) and cavity and anneal$4 and transistor and transducer and (dielectric or oxide) and (argon or nitrogen or xenon or helium) and atmospher	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/10/13 08:15

EAST Search History

S13	29	((semiconductor or substrate or wafer or chip) near8 (trench$2)) and cavity and anneal$4 and transistor and transducer and (dielectric or oxide) and (argon or nitrogen or xenon or helium) and atmosphere	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/10/13 08:57
S14	0	((semiconductor or substrate or wafer or chip) near8 (trench$2)) and cavity and anneal$4 and transistor and transducer and (dielectric or oxide) and (argon or nitrogen or xenon or helium) and atmosphere and epitaxy	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/10/13 08:15
S15	0	((semiconductor or substrate or wafer or chip) near8 (trench$2)) and cavity and anneal$4 and transistor and transducer and (dielectric or oxide) and (argon or nitrogen or xenon or helium) and atmosphere and "SOI"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/10/13 08:44
S16	190	"5324683"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/10/13 08:45
S17	168	"5324683"	USPAT	OR	ON	2005/10/13 08:45
S18	44	((semiconductor or substrate or wafer or chip) near8 (trench$2 or slot$2 or hole$2)) and cavity and anneal$4 and transistor and transducer and (dielectric or oxide) and (argon or nitrogen or xenon or helium) and atmosphere	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/10/13 09:14
S19	1	((semiconductor or substrate or wafer or chip) near8 (trench$2 or slot$2 or hole$2)) and cavity and anneal$4 and transistor and transducer and (dielectric or oxide) and (argon or nitrogen or xenon or helium) and atmosphere and epitaxy	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/10/13 08:58
S20	29	((semiconductor or substrate or wafer or chip) near8 (trench$2 or slot$2 or hole$2)) and cavity and anneal$4 and transistor and transducer and (dielectric or oxide) and (argon or nitrogen or xenon or helium) and atmosphere and epitax$4	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/10/13 11:47

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S21	9508070	DE "10131249" A1	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/10/13 11:48
S22	0	("DE10131249A1").PN.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2005/10/13 11:49
S23	0	("DE10131249A1").PN.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2005/10/13 11:49
S24	0	("10131249A1").PN.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2005/10/13 11:49
S25	4	("10131249").PN.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2005/10/13 11:58
S26	0	(2004/0142542A1).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2005/10/13 11:59
S27	0	2004/0142542	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2005/10/13 11:59
S28	0	"2004/0142542 A1"	US-PGPUB	OR	OFF	2005/10/13 11:59
S29	1	("0142542").PN.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2005/10/13 12:00
S30	0	(2004/0142542).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2005/10/13 12:01
S31	0	(US2004/0142542).CCLS.	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2005/10/13 12:03
S32	2	"20040142542"	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2005/10/13 12:36

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S33	1	"SOI" and "porous silicon" and (dielectric or oxide) and transistor and microphone and transducer	US-PGPUB; USPAT; EPO; JPO; DERWENT	OR	OFF	2005/10/13 12:38
S34	523	"SOI" and "porous silicon" and (dielectric or oxide) and (transistor or microphone or transducer)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/10/13 12:38
S35	8	"SOI" and "porous silicon" and (dielectric or oxide) and (transistor and microphone)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/10/13 12:39
S36	6	"SOI" and "porous silicon" and (dielectric or oxide) and (transistor and transducer)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/10/13 12:39
S37	595	"SOI" and ((semiconductor or wafer or substrate) near8 trench$2) and cavity and (dielectric or oxide or insulat$4) and silicon	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/23 14:47
S38	16	"SOI" and ((semiconductor or wafer or substrate) near8 trench$2) and cavity and (dielectric or oxide or insulat$4) and silicon and anneal$4 and oxidiz$4 and atmosphere and "MOSFET"	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/23 14:55
S39	0	"SOI" and ((semiconductor or wafer or substrate) near8 trench$2) and cavity and (dielectric or oxide or insulat$4) and silicon and anneal$4 and oxidiz$4 and atmosphere and "MOSFET" and (257/288.ccls.)	US-PGPUB; USPAT; USOCR; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/06/23 14:56
S40	0	SOI and (substrate or semiconductor or wafer or carrier or chip) near4 (trench$4 or via$4 or hole$4 or opening$4) and (porous near4 silicon) and epiatx$4 and cavit$3 and (anneal$4 or heat$4 or thermal$4) and MOSFET and device and (dielectric or oxide or insulat$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/30 08:21

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S41	0	SOI and (substrate or semiconductor or wafer or carrier or chip) near4 (trench$4 or via$4 or hole$4 or opening$4) and (porous near4 silicon) and epiatx$4 and cavit$3 and (anneal$4 or heat$4 or thermal$4) and (dielectric or oxide or insulat$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/30 08:22
S42	0	SOI and (substrate or semiconductor or wafer or carrier or chip) near4 (trench$4 or via$4 or hole$4 or opening$4) and (porous near4 silicon) and epiatx$4 and cavit$3 and (anneal$4 or heat$4 or thermal$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/30 08:22
S43	0	(substrate or semiconductor or wafer or carrier or chip) near4 (trench$4 or via$4 or hole$4 or opening$4) and (porous near4 silicon) and epiatx$4 and cavit$3 and (anneal$4 or heat$4 or thermal$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/30 08:23
S44	0	(substrate or semiconductor or wafer or carrier or chip) near9 (trench$4 or via$4 or hole$4 or opening$4) and (porous near4 silicon) and epiatx$4 and cavit$3 and (anneal$4 or heat$4 or thermal$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/30 08:23
S45	553445	(substrate or semiconductor or wafer or carrier or chip) near9 (trench$4 or via$4 or hole$4 or opening$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/30 08:24
S46	2840	(substrate or semiconductor or wafer or carrier or chip) near9 (trench$4 or via$4 or hole$4 or opening$4) and (porous near4 silicon)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/30 08:24
S47	608	(substrate or semiconductor or wafer or carrier or chip) near9 (trench$4 or via$4 or hole$4 or opening$4) and (porous near4 silicon) and cavit$4	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/30 08:25

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S48	240	(substrate or semiconductor or wafer or carrier or chip) near9 (trench$4 or via$4 or hole$4 or opening$4) and (porous near4 silicon) and cavit$4 and epitax$4 and (dielectric or oxide or insulat$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/30 08:27
S49	16	(substrate or semiconductor or wafer or carrier or chip) near9 (trench$4 or via$4 or hole$4 or opening$4) and (porous near4 silicon) and (buried near4 cavit$4) and epitax$4 and (dielectric or oxide or insulat$4)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/30 10:26
S50	11	(substrate or semiconductor or wafer or carrier or chip) near9 (trench$4 or via$4 or hole$4 or opening$4) and (porous near4 silicon) and (buried near4 cavit$4) and epitax$4 and (dielectric or oxide or insulat$4) and SOI	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/30 08:27
S51	5	(substrate or semiconductor or wafer or carrier or chip) near9 (trench$4 or via$4 or hole$4 or opening$4) and (porous near4 silicon) and (buried near4 cavit$4) and epitax$4 and (dielectric or oxide or insulat$4) and SOI and MOSFET	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/30 08:34
S52	11	(substrate or semiconductor or wafer or carrier or chip) near9 (trench$4 or via$4 or hole$4 or opening$4) and (porous near4 silicon) and (buried near4 cavit$4) and epitax$4 and (dielectric or oxide or insulat$4) and SOI	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/30 08:34